

**METHOD OF FABRICATING A NON-VOLATILE MEMORY DEVICE HAVING
A TUNNEL-INSULATING LAYER INCLUDING MORE THAN TWO PORTIONS
OF DIFFERENT THICKNESS**

ABSTRACT OF THE DISCLOSURE

A method of fabricating a non-volatile memory device, which has a tunnel insulating layer consisting of two or more portions of different thickness, cell transistors, and auxiliary transistors for applying external voltage and for interfacing with peripheral circuits is described. According to the method, the tunnel insulating layer, a conductive layer, and a first insulating layer are sequentially deposited over a semiconductor substrate. The resultant structure is selectively etched to a given depth to form trenches. A second insulating layer is deposited over the substrate including the trenches, and the second insulating layer is selectively removed so as to form element isolation regions consisting of the trenches filled with the second insulating layer. The first insulating layer is selectively removed, and the second insulating layer is selectively removed by a CMP process to expose the conductive layer. The conductive layer is used as the stopping layer during the CMP process.

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